TEXAS INSTRUMENTS

A 5-V Input, 1.8-V Output, 6-A Synchronous Buck Converter

User's Guide

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1 Introduction

The TPS40041EVM-001 evaluation module (EVM) is a synchronous buck converter providing a fixed 1.8-V output at up to 6 A from a 5-V input bus or 3 A from a 3.3-V input. The EVM is designed to start up from a single supply, so no additional bias voltage is required for start-up. The module uses the TPS40041 Reduced Pin Count Low-Voltage Synchronous Buck Controller.

1.1 Description

TPS40041EVM-001 is designed to use a regulated 5-V (4.5 V to 5.5 V) or 3.3-V (3.0 V to 3.6 V) bus to produce a medium current, regulated 1.8-V output at up to 6 A of load current. TPS40041EVM-001 is designed to demonstrate the TPS40041 in a typical regulated bus to low-voltage application while providing a number of test points to evaluate the performance of the TPS40041 in a given application. The EVM can be modified to support output voltages from 0.9 V to 2.5 V by changing a single set resistor.

1.2 Applications

- Non-isolated medium current point of load and low voltage bus converters.
- Networking equipment
- Telecommunications equipment
- Computer peripherals
- Digital set top box

1.3 Features

- 3.0-V to 5.5-V input range
- 1.8-V fixed output, adjustable with single resistor
- 6-A_{DC} steady state output current (3 A at 3.3-V input)
- 600-kHz switching frequency (fixed by TPS40041)
- Single SO-8 dual MOSFET for both main switch and synchronous rectifier.
- Double sided 2-layer PCB with all components on top side
- Active converter uses less than 1 square inch < 1.0" x 1.0"
- Convenient test points for probing switching waveforms and non-invasive loop response testing

2 TPS40041EVM-001 Electrical Performance Specifications

Table 1. TPS40041EVM-001 Electrical and Performance Specifications

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Input Characteristics						
Input Voltage Range			3.0		5.5	V
Max Input Current	VIN = 4.5V, IOUT = 6A			2		A
	VIN = 3V, IOUT = 3A			2		
No-Load Input Current	VIN = 5.5V, IOUT = 0A			100		mA
Output Characteristics						
Output Voltage	R6 = 10k R5 = OPEN		1.75	1.80	1.85	V
Output Voltage Regulation	Line Regulation (3.0V<VIN<5.5V, IOUT = 2A)				0.2%	
	Load Regulation (0A<IOUT<6A, VIN = 5V)				0.2%	
Output Voltage Ripple	VIN = 5.5V, IOUT = 6A			10	36	mVpp
Output Load Current	VIN = 4.5 – 5.5V		0		6	A
	VIN = 3.0 – 3.6V		0		3	
Short Circuit Input Current	VIN = 5.5V VOUT = 0V			6		mA
System Characteristics						
Switching Frequency			500	600	700	kHz
Peak Efficiency	VOUT = 1.8V, 1A<IOUT<4Av	VIN = 3.0V		93%		
		VIN = 4.5V		91%		
		VIN = 5.5V		90%		
Full Load Efficiency	VOUT = 1.8V, IOUT = 3A	VIN = 3.0V		91%		
	VOUT = 1.8V, IOUT = 6A	VIN = 4.5V		89%		
		VIN = 5.5V		88%		

3 Schematic

Figure 1. TPS40041EVM-001 Schematic

Note: For reference only, see Table 4 List of Materials for specific values.

3.1 Adjusting Output Voltage (R5)

The regulated output voltage can be adjusted within a limited range by changing the ground resistor in the feedback resistor divider (R5). The output voltage is given by the formula:

$$V_{OUT} = V_{REF} \times \frac{R8 + R5}{R5}$$

Where V_{VREF} = 0.600 V and R8 = 20 KΩ

Table 2 contains common values for R1 to generate popular output voltages. TPS40041EVM-001 is stable through these output voltages but the efficiency may suffer as the power stage is optimized for the 1.8-V output.

Table 2. Adjusting V$_{OUT}$ with R5

V$_{OUT}$	R5
2.5 V	6.34 kΩ
2.25 V	7.32 kΩ
2.0 V	8.66 kΩ
1.8 V	10 kΩ
1.5 V	13.3 kΩ
1.2 V	20 kΩ
1.0 V	30 kΩ
0.9 V	40 kΩ

The values in Table 2 provide less than 1% nominal set-point error in the output voltage. If a tighter nominal value is required, R4 can be used in parallel with R5 to obtain a wider range of resistor values using commonly available E96 resistors.

3.2 Adjusting Short Circuit Protection (R6)

The TPS40041 uses a selectable current limit for short circuit protection. The current limit is selected from three levels by placing a resistor at R6. The TPS40041 compares the voltage drop across the high-side FET (VDD to SW) to an internal reference voltage selected during start-up. The voltage levels are shown in Table 3.

Table 3. Adjusting V$_{SCP}$ with R6

V$_{SCP}$	R6
105 mV	2.4 kΩ
180 mV	OPEN
300 mV	12 kΩ

The current before declaring short circuit protection can be determined by dividing the $V_{SC}P$ by the $R_{DS(on)}$ of the high-side FET (Q2).

3.3 Enable (TP1 & SW1)

TPS40041EVM-001 provides an active high enable input (TP1) to allow the user to evaluate the TPS40041's enable function. The enable test point uses a 100-kΩ pull-up resistor so TPS40041 turns on if the enable test point is left floating.

4 Test Set Up

4.1 Equipment

4.1.1 Voltage Source

The input voltage source (V_{IN}) should be a 0 V to 6 V variable dc source capable of 5 A_{DC}. Connect V_{IN} to J1 as shown in Figure 3.

4.1.2 Meters

- **A1:** 0 A_{DC} to 5 A_{DC}, ammeter
- **V1:** V_{IN} 0 V to 15 V, voltmeter
- **V2:** V_{OUT} 0 V to 15 V, voltmeter

4.1.3 Loads

- LOAD1

The output load, LOAD1, should be an electronic constant current mode load capable of 0 A_{DC} to 6 A_{DC} at 1.8 V.

4.1.4 Oscilloscope

A digital or analog oscilloscope can be used to measure the ripple voltage on V_{OUT}. The oscilloscope should be set for 1-MΩ impedance, 20-MHz bandwidth, ac coupling, 1-μs/div. horizontal resolution and 10-mV/div. vertical resolution for taking output ripple measurements. TP 14 and TP 15 can be used to measure the output ripple voltage by placing the oscilloscope probe tip through TP14 and holding the ground barrel to TP15 as shown in Figure 3. For a hands free approach, the loop in TP15 can be cut and opened to cradle the probe barrel. Using a leaded ground connection may induce additional noise due to the large ground loop area.

4.1.5 Recommended Wire Gauge

- V_{IN} to J1

The connection between the source voltage, VIN and J1 of HPA137 can carry as much as 3 A_{DC}. The minimum recommended wire size is AWG #16 with the total length of wire less than 4 feet, 2 feet input, 2 feet return.

- J2 to LOAD1 (power)

The power connection between J2 of HPA137 and LOAD1 can carry as much as 6 A_{DC}. The minimum recommended wire size is 2 x AWG #16, with the total length of wire less than 4 feet, 2 feet output, 2 feet return.

4.1.6 Other

- Fan

This evaluation module includes components that can get hot to the touch, because this EVM is not enclosed to allow probing of circuit nodes, a small fan capable of 200 lfm to 400 lfm is required to reduce component surface temperatures to prevent user injury. The EVM should not be left unattended while powered. The EVM should not be probed while the fan is not running.

4.2 Equipment Setup

Shown in Figure 3 is the basic test set up recommended to evaluate the TPS40041EVM-001. Please note that although the return for J1 and J2 are the same, the connections should remain separate as shown in Figure 2.

4.2.1 Procedure

1. Working at an ESD workstation, make sure that any wrist straps, bootstraps or mats are connected referencing the user to earth ground before power is applied to the EVM. Electrostatic smock and safety glasses should also be worn.
2. Prior to connecting the dc input source, V_{IN}, it is advisable to limit the source current from V_{IN} to 5.0 A maximum. Make sure V_{IN} is initially set to 0 V and connected as shown in Figure 2.
3. Connect the ammeter A1 (0 A to 5 A range) between V_{IN} and J1 as shown in Figure 2.
4. Connect voltmeter V1 to TP1 and TP2 as shown in Figure 2.
5. Connect LOAD1 to J2 as shown in Figure 2. Set LOAD1 to constant current mode to sink 0 A_{DC} before V_{IN} is applied.
6. Connect voltmeter, V2 across TP14 and TP15 as shown in Figure 2.
7. Connect Oscilloscope probe to TP14 and TP15 as shown in Figure 3.
8. Place fan as shown in Figure 2 and turn on, making sure air is flowing across the EVM.
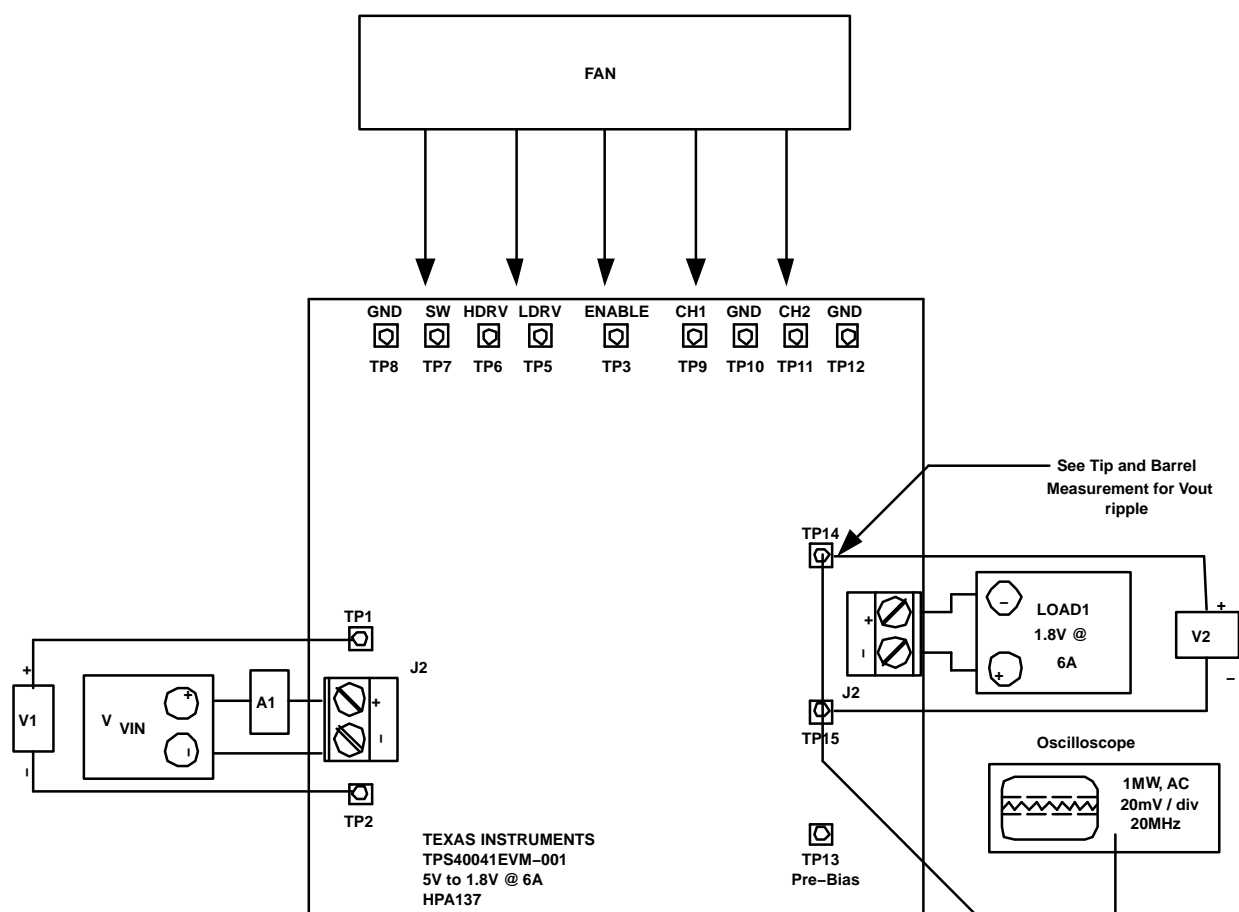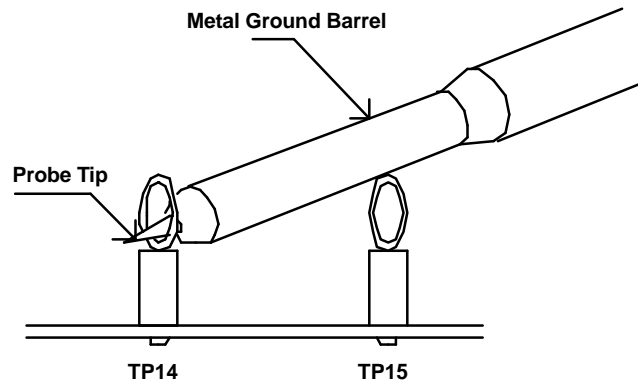
4.2.2 Diagram

Figure 2. TPS40041EVM-001 Recommended Test Set-Up

Tip and Barrel Vout ripple measurement

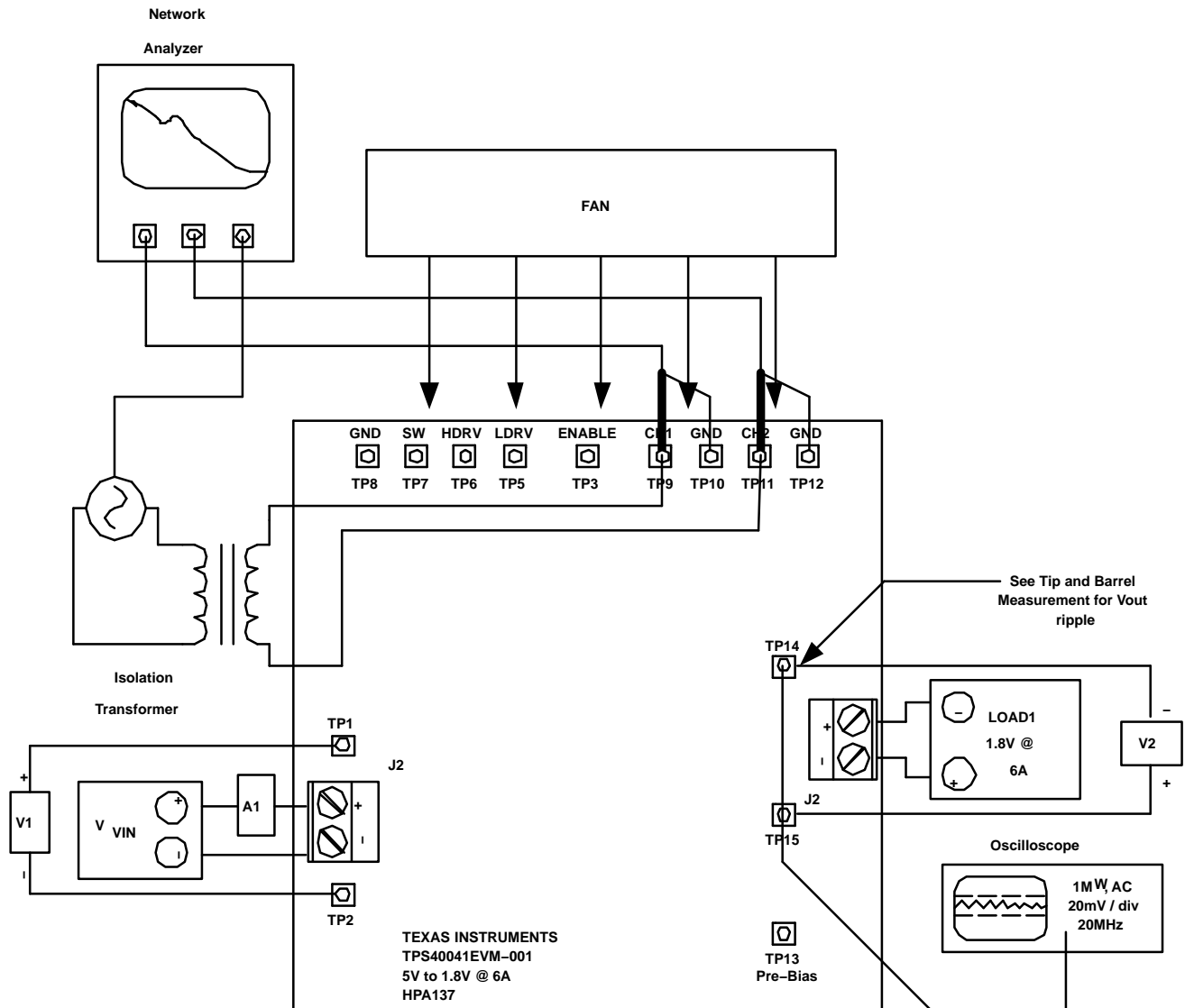**Figure 3. Output Ripple Measurement - Tip and Barrel using TP9 and TP10**

Figure 4. Control Loop Measurement Setup

4.3 Start-Up / Shut-Down Procedure

1. Increase V_{IN} from 0 V_{DC} to 5 V_{DC}.
2. Vary LOAD1 from 0 V_{DC} to 6 V_{DC}.
3. Vary V_{IN} from 3.0 V_{DC} to 5.5 V_{DC}.
4. Decrease LOAD1 to 0 A.

4.4 Control Loop Gain and Phase Measurement Procedure

1. Connect 1-kHz to 1-MHz isolation transformer to TP9 and TP11 as show in Figure 4.
2. Connect input signal amplitude measurement Probe (Channel A) to TP9 as shown in Figure 4.
3. Connect output signal amplitude measurement probe (Channel B) to TP11 as shown in Figure 4.
4. Connect ground lead of Channel A and Channel B to TP10 & TP12 as shown in Figure 4.
5. Inject 25 mV or less signal across R7 through isolation transformer.
6. Sweep frequency from 1 kHz to 1 MHz with 10 Hz or lower post filter.
7. Control loop gain can be measured by: $20 \times \log\left(\dfrac{ChannelB}{ChannelA}\right)$
8. Control loop phase is measured by the phase difference between Channel A and Channel B.
9. Disconnect isolation transformer from TP9 and TP11 before making other measurements, signal Injection into feedback may interfere with accuracy of other measurements.

4.5 Equipment Shutdown

1. Shut down oscilloscope
2. Shut down LOAD1
3. Shut down V_{IN}
4. Shut down FAN

5   TPS40041EVM Typical Performance Data and Characteristic Curves

Figure 5 through Figure 9 present typical performance curves for the TPS40041EVM-001. Since actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and may differ from actual field measurements.
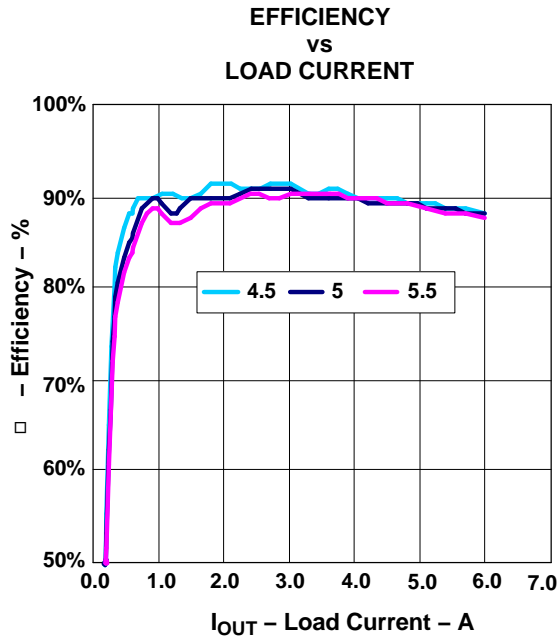
5.1   *Efficiency*

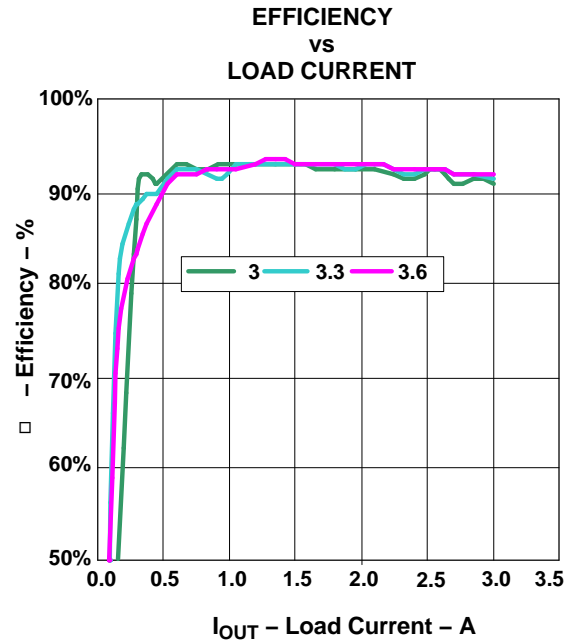**Figure 5. TPS40041EVM-001 Efficiency V$_{IN}$ = 4.5 V to 5.5 V, V$_{OUT}$ = 1.8 V, I$_{OUT}$ = 0 A to 6 A**

Figure 6. TPS40041EVM-001 Efficiency V$_{IN}$ = 3.0 V to 3.6 V, V$_{OUT}$ = 1.8 V, I$_{OUT}$ = 0 A to 3 A
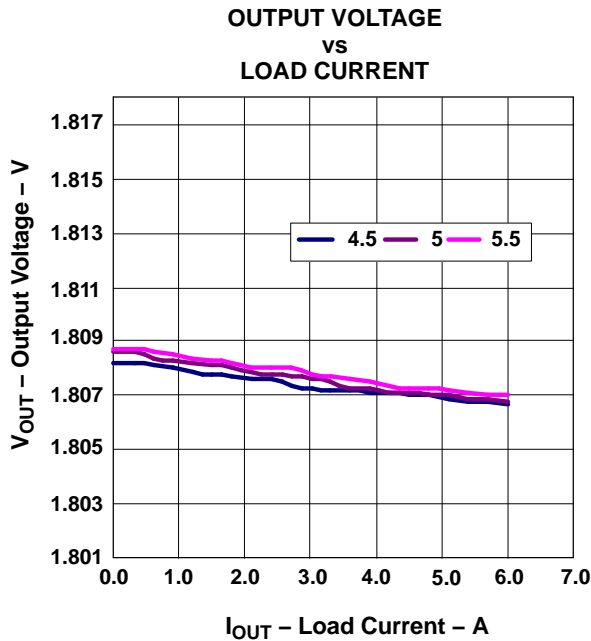
5.2   *Line and Load Regulation*

**OUTPUT VOLTAGE
vs
LOAD CURRENT**

Figure 7. TPS40041EVM-001 Line and Load Regulation V_{IN} = 4.5 V to 5.5 V, V_{OUT} = 1.8 V, I_{OUT} = 0 A to 6 A

**EFFICIENCY
vs
LOAD CURRENT**

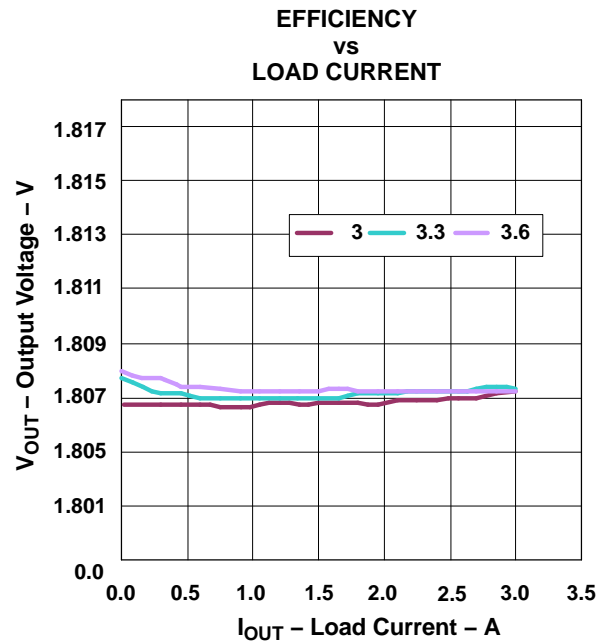**Figure 8. TPS40041EVM-001 Line and Load Regulation V_{IN} = 3.0 V to 3.6 V, V_{OUT} = 1.8 V, I_{OUT} = 0 A to 3 A**

5.3   *Output Voltage Ripple*
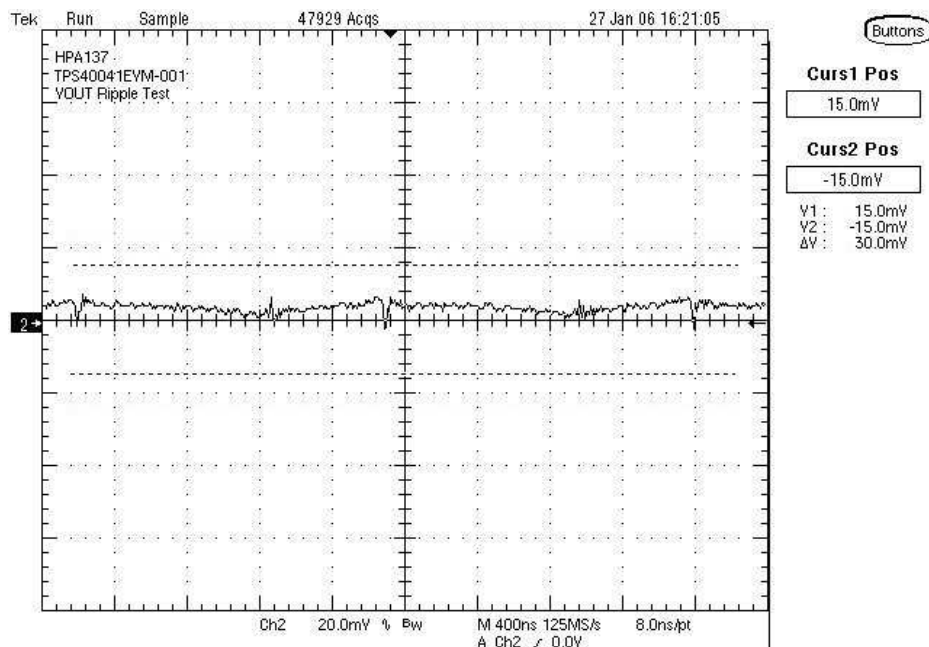
Figure 9. TPS40041EVM-001 Output Voltage Ripple, V_{IN} = 5.5V, I_{OUT} = 6 A

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6   EVM Assembly Drawings and Layout

The following figures, Figure 10 through Figure 13, show the design of the TPS40041EVM-001 printed circuit board. The EVM has been designed using a double sided, 2-oz copper-clad circuit board 2.5" x 2.4" with all components in a 1" x 1" active area on the top side to allow the user to easily view, probe and evaluate the TPS40041 control device in a practical application. Moving components to both sides of the PCB or using additional internal layers can offer additional size reduction for space constrained systems.
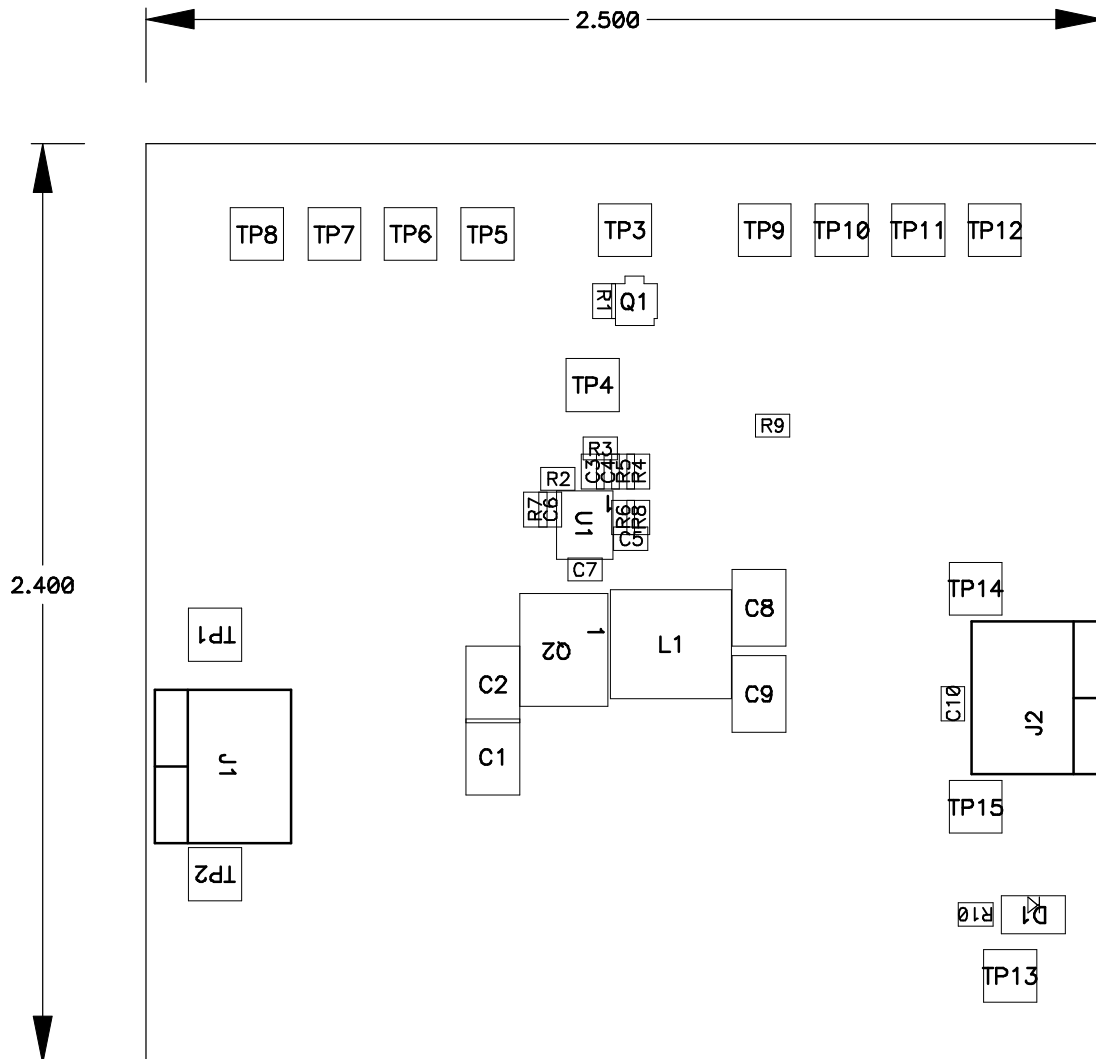
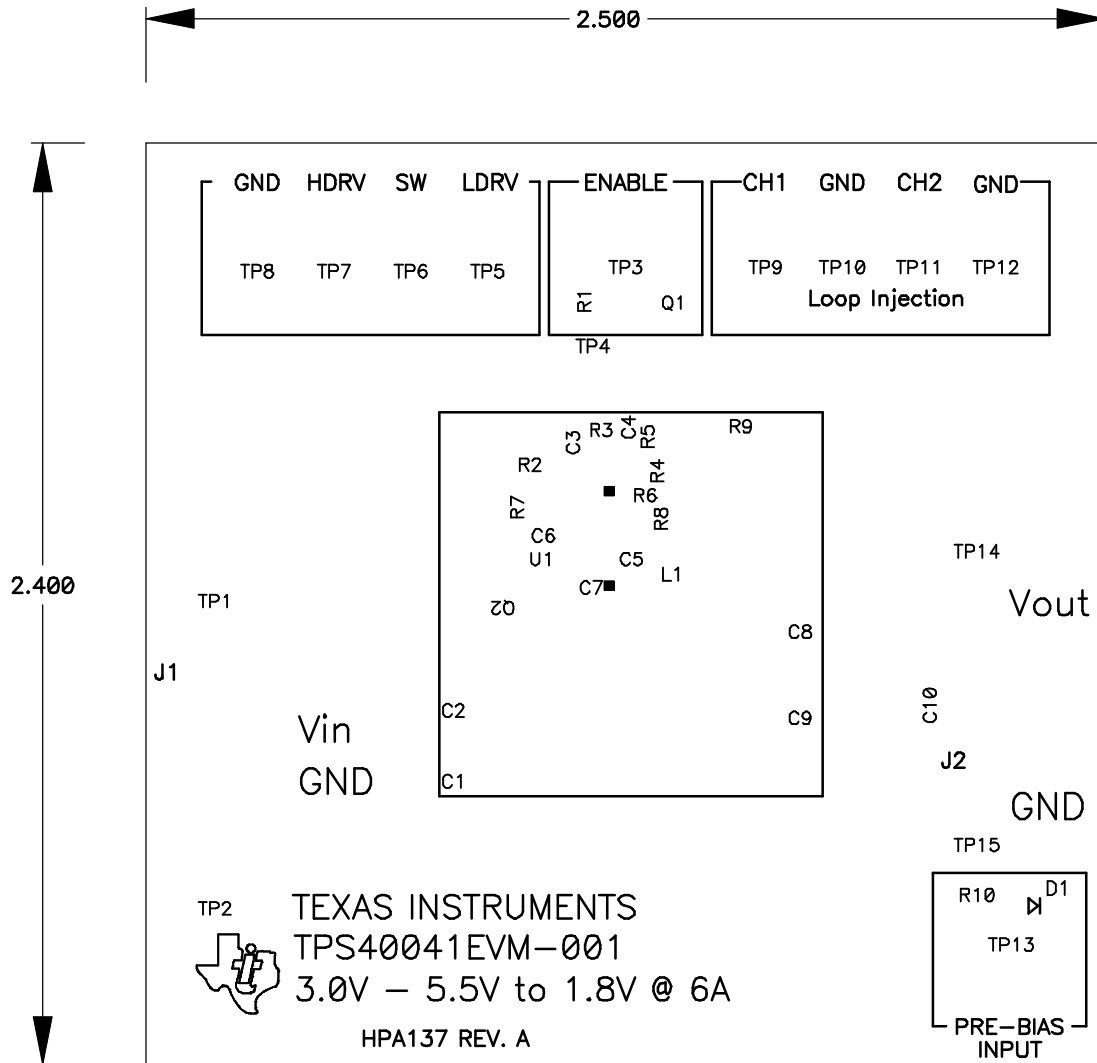**Figure 10. TPS40041EVM-001 Component Placement, Top View**
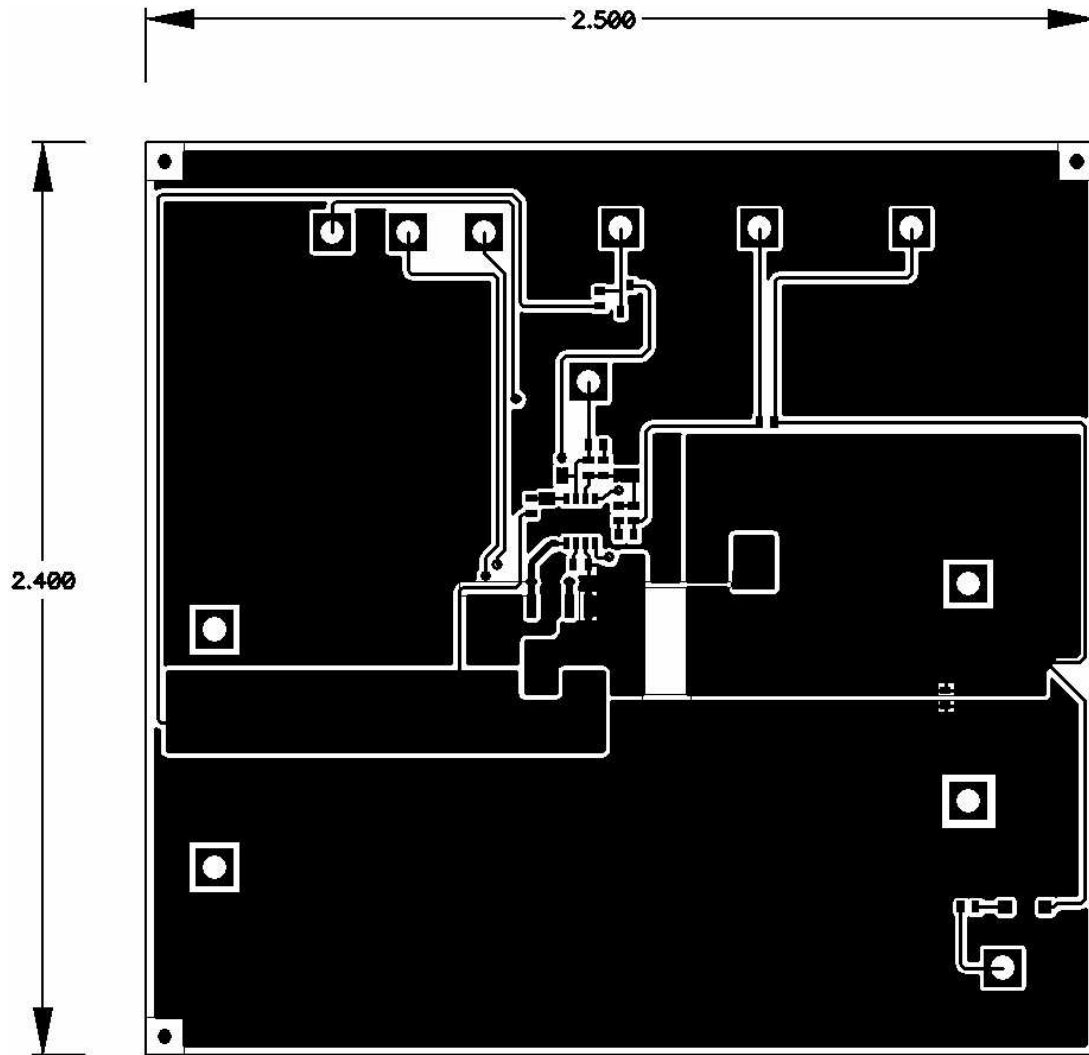
Figure 11. TPS40041EVM-001 Silkscreen, Top View

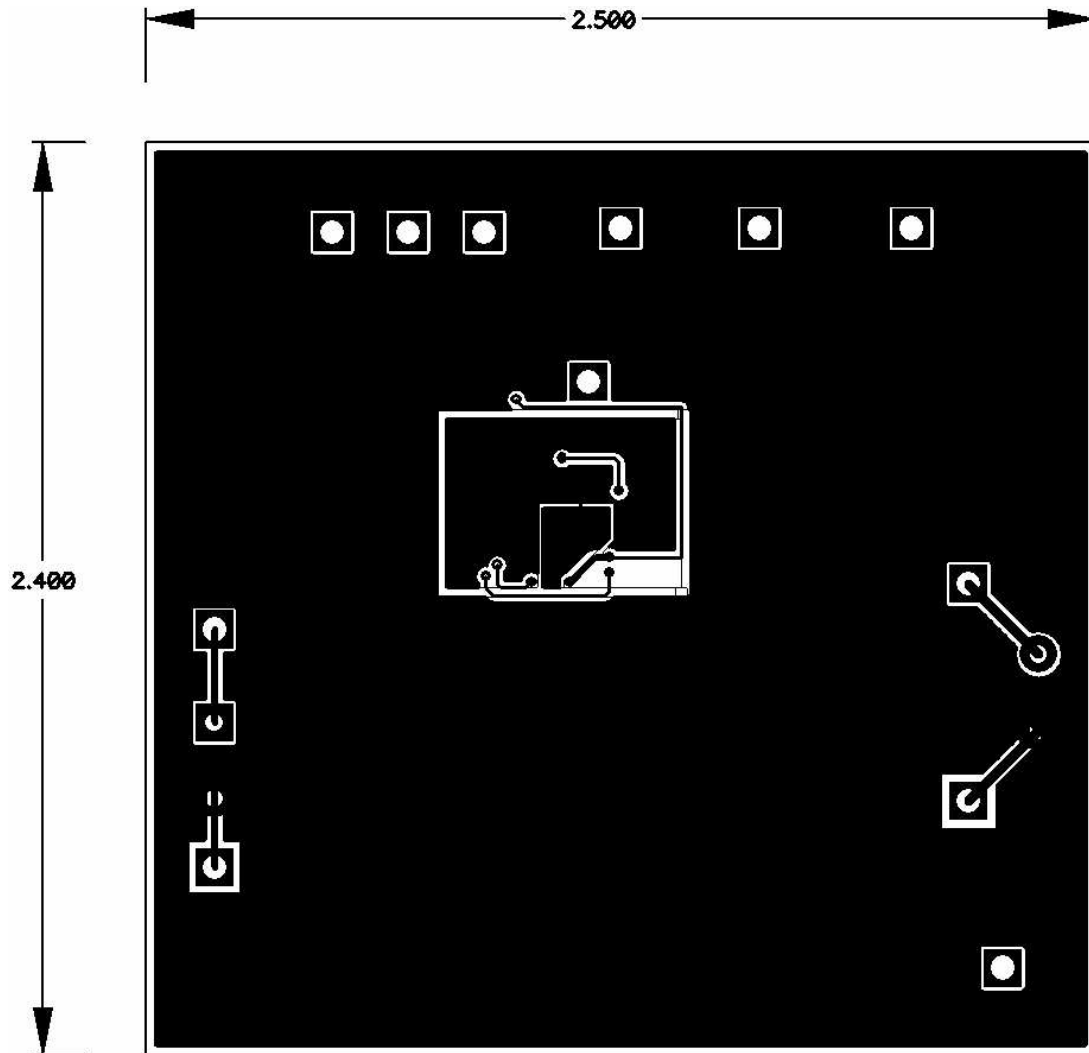**Figure 12. TPS40041EVM-001 Top Copper, Top View**

Figure 13. TPS40041EVM-001 Bottom Copper, X-Ray View from Top

7   LIST OF MATERIALS

Table 4 lists the EVM components as configured according to the schematic shown in Figure 1.

Table 4. TPS40041EVM-001 List of Materials

REF	COUNT	DESCRIPTION	MANUFACTURER	PART NUMBER
C1, C2, C8, C9	4	Capacitor, ceramic, 6.3 V, X5R, 20%, 100 µF, 1210	TDK	C3225X5R0J107M
C3	1	Capacitor, ceramic, 50 V, X7R, 20%, 220 pF, 0402	TDK	C1005X7R1H221M
C4	1	Capacitor, ceramic, 50 V, X7R, 20%, 2200 pF, 0402	TDK	C1005X7R1H222M
C5	1	Capacitor, ceramic, 50 V, X7R, 20%, 1000 pF, 0402	TDK	C1005X7R1H102M
C6, C10	2	Capacitor, ceramic, 6.3 V, X5R, 20%, 1.0 µF, 0402	TDK	C1005X5R0J105M
C7	1	Capacitor, ceramic, 6.3 V, X5R, 20%, 0.22 µF, 0402	TDK	C1005X5R0J224M
D1	1	Diode, schottky, 200 mA, 30 V, SOD323	On Semi	BAT54HT1
J1, J2	2	Terminal block, 2 pin, 15 A, 5.1 mm 0.40 x 0.35 inch	OST	ED1609
L1	1	Inductor, SMT, 1.0 µH, 12 A, 6.6 mΩ, 1.0 µH, 0.268 x 0.268 inch	Pulse	PG0083.102
Q1	1	MOSFET, N-channel, VDS 60 V, RDS 2 Ω, ID 115 mA SOT-323 (SC-70)	Diodes Inc	2N7002W-7
Q2	1	MOSFET, dual N-channel, 12 V, 10 A, 15 mΩ SO8	IR	IRF7910
R1	1	Resistor, chip, 100 kΩ, 1/16 W, 1% 0402	Std	Std
R10	1	Resistor, chip, 100 Ω, 1/16 W, 1% 0402	Std	Std
R2, R4	0	Resistor, chip, 1/16 W, OPEN, 0402	Std	Std
R3	1	Resistor, chip, 7.15 kΩ, 1/16 W, 1% 0402	Std	Std
R5	1	Resistor, chip, 10.0 kΩ, 1/16 W, 1% 0402	Std	Std
R6	1	Resistor, chip, 6.34 kΩ, 1/16 W, 1% 0402	Std	Std
R7	1	Resistor, chip, 1 Ω, 1/16 W, 1% 0402	Std	Std
R8	1	Resistor, chip, 20 kΩ, 1/16 W, 1% 0402	Std	Std
R9	1	Resistor, chip, 49.9 Ω, 1/16 W, 1% 0402	Std	Std
TP1, TP14	2	Test point, red, thru hole 0.125 x 0.125		5010
TP2, TP8, TP10, TP12, TP15	5	Test point, black, thru hole 0.125 x 0.125		5011
TP3, TP4, TP5, TP6, TP7, TP9, TP11, TP13	8	Test point, white, thru hole 0.125 x 0.125		5012
U1*	1	TPS40041DRB, Low Voltage DC/DC Synchronous Buck Controller, QFN-8P	TI	TPS40041DRB

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